What is Claimed is:

[c1] A method for qualifying a leakage current to be tolerable or not, the leakage current being present in a first test area of a hardware circuit which comprises said first test area between a first node and a second node being able to be forced to a predefined voltage potential, the method comprising the steps of:

a) shutting off any operational current flow into said first test area,

b) generating an evaluable voltage difference between said first node and said second node being characteristic for said leakage current to provide a resulting voltage at said first node, and

c) qualifying said leakage current as tolerable or not in dependence of the resulting voltage at said first node.

[c2] The method according to claim 1, wherein said leakage current flows in a test path comprising a switching element acting as an Ohm-resistor having a predetermined operational resistance, and said test area being connected in series to said resistor.

[c3] The method according to claim 2, wherein said resistor is a transistor switched in pass mode.

[c4] The method according to claim 1, wherein said first node is a tap node between two transistors of a driver stage, forming a voltage divider.

[c5] The method according to claim 4, wherein a test region comprising said first test area and a second test area includes a receiver device of a combined driver/receiver stage of a semiconductor chip.

[c6] The method according to claim 5, wherein said test region is used for qualifying and/or quantifying the leakage current in a signal input/output book of a semiconductor chip.

[c7] A hardware circuit for qualifying a leakage current to be tolerable or not, the hardware circuit comprising:

a) a leakage test area between a first node and a second node, the second node arranged to be forced to a predefined voltage potential,

b) a first device for shutting off any operational current flow into at least

said leakage test area,

c) a second device for generating an evaluable voltage difference between said first node and said second node being characteristic for said leakage current to provide a resulting voltage at said first node, and

d) a third device for qualifying and/or quantifying said leakage current as tolerable or not in dependence of the resulting voltage at said first node.

[c8] The hardware circuit according to claim 7, wherein said first node is implemented as a tap node of a voltage divider.

[c9] The hardware circuit according to claim 8, wherein said voltage divider comprises a first and a second transistor connected in series, and said tap node is connected between the drain of the first transistor and the source of the second transistor, the gate of each of said first and second transistors being connected to selectively run two different test modes, in each of which a respective other transistor is switched in pass mode and forms part of the test path when the respective other transistor is switched in lock mode.

[c10] The hardware circuit according to claim 9, wherein the circuit is arranged as a combined input/output stage of a semiconductor chip having a driving P-device comprising a plurality of P- type transistors and a driving N-device comprising a second plurality of N-type transistors, said driving P-device and said driving N-device being connected in series between a first voltage level and a second voltage level, said drive devices driving high, low, and HZ states to a terminal pad connecting off from the semiconductor chip, the circuit further comprising a receiving device connected in parallel to said terminal pad, wherein when an electrical resistance of one of said first and second transistors in pass mode is implemented as R = (VDD - VH) / Ileakmax, where R represents the electrical resistance of said one transistor in pass mode, VDD represents the supply voltage, VH represents a voltage at said pad terminal, and Ileakmax represents a maximum allowed leakage current of said one transistor in pass mode, the receiving device is prevented from switching when coming from initial-state to test-state of said input/output stage.

[c11] The hardware circuit according to claim 9, wherein the circuit is arranged as a

combined input/output stage of a semiconductor chip having a driving P-device comprising a plurality of P- type transistors and a driving N-device comprising a second plurality of N-type transistors, said driving P-device and said driving N-device being connected in series between a first voltage level and a second voltage level, said drive devices driving high, low, and HZ states to a terminal pad connecting off from the semiconductor chip, the circuit further comprising a receiving device connected in parallel to said terminal pad, wherein when an electrical resistance of one of said first and second transistors in pass mode is implemented as R = VL / Ileakmax, where R represents the electrical resistance of said one transistor in pass mode, VL represents a voltage at said pad terminal, and Ileakmax represents a maximum allowed leakage current of said one transistor in pass mode, the receiving device is prevented from switching when coming from lower resistance values associated with the pass mode of said input/output stage.

[c12] The hardware circuit according to claim 7, wherein the circuit is used in a semiconductor chip.

[c13] The hardware circuit according to claim 7, wherein the circuit is used in a semiconductor chip module.

[c14] The hardware circuit according to claim 7, wherein the circuit is used in a semiconductor multi-chip module.

[c15] The hardware circuit according to claim 7, wherein the circuit is used in a printed circuit board.

[c16] A computer program product for execution in a data processing system comprising computer program code portions for performing respective steps of a method for qualifying a leakage current to be tolerable or not, the leakage current being present in a first test area of a hardware circuit which comprises said first test area between a first node and a second node being able to be forced to a voltage potential of a predefined value, when said computer program code portions are executed on a computer, the method comprising the steps of:

a) shutting off any operational current flow into said test area,

b) generating an evaluable voltage difference between said first node and said second node being characteristic for said leakage current to provide a resulting voltage at said first node, and

c) qualifying said leakage current as tolerable or not in dependence of the resulting voltage at said first node.

[c17] A computer program product stored on a computer usable medium comprising computer readable program code portions for causing a computer to perform a method for qualifying a leakage current to be tolerable or not, the leakage current being present in a first test area of a hardware circuit which comprises said first test area between a first node and a second node being able to be forced to a voltage potential of a predefined value, when said computer readable program code portions are executed on a computer, the method comprising the steps of:

a) shutting off any operational current flow into said test area,

b) generating an evaluable voltage difference between said first node and said second node being characteristic for said leakage current to provide a resulting voltage at said first node, and

c) qualifying said leakage current as tolerable or not in dependence of the resulting voltage at said first node.